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| **Course Name:** | **Digital Electronics (116U02C304)** | **Semester:** | **III** |
| **Date of Performance:** |  | **Batch No:** |  |
| **Faculty Name:** |  | **Roll No:** |  |
| **Faculty Sign & Date:** |  | **Grade/Marks:** |  |

# Experiment No: 5

**Title: Multiplexer**

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| **Aim and Objective of the Experiment:** |
| Implementation of MUX using MSI IC andImplementation of function using decoder IC |

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| **COs to be achieved:** |
| **CO2:** Design combinational logic circuits using MSI devices |

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| **Theory:** |
| **Multiplexer:**A multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2n inputs has n select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. |

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| **Circuit Diagram/ Block Diagram:** |  |
|  | **S1** | **S0** | **Q** |  |
| 0 | 0 | d00 |
| 0 | 1 | d01 |
| 1 | 0 | d10 |
| 1 | 1 | d11 |

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| http://www.toves.org/books/comps/mux-circ.png4: 1 Multiplexer | **Q = S1’S0’d00+S1’S0d01+S1S0’d10+S1S0d11** |
| **Decoder**: A decoder is a combinational circuit with n inputs and at most 2n outputs. They may be used to route input data to a specified output line, as, for example, is done in memory addressing, where input data are to be stored in (or read from) a specified memory location. They can be used for some code conversions. Or they may be used for data distribution i.e. demultiplexing. |
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| **Stepwise-Procedure:** |
| 1. Implement a function F (A, B, C) = ∑m (0, 1, 3, ,7) using single 8:1 mux
2. Implement a function F (A, B, C) = ∑m (0, 3, 4, 7) using single 4:1 mux and additional gates if required
3. Implement 3 to 8 decoder for the given function (will be given by the faculty)
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| **Post Lab Subjective/Objective type Questions:** |
| 1. Implement full adder Sum(A,B,Cin) and Cout(A,B,Cin) with
	1. Two 8:1 multiplexers
	2. Two 4:1 multiplexers
2. There are four adjacent parking slot in a company. Each slot is equipped with a sensor whose output is asserted low when a car is occupying a slot, otherwise sensor output is high. Design and draw a schematic for a system, which will generate a low output if and only if there are two or more than two adjacent slots vacant

Implement it using 8: 1 mux1. Implement F(A,,B,C) = ∑m (0, 1, 3, ,7) using 74138 IC and two input NAND gates
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**Conclusion:**

**Signature of faculty in-charge with Date:**