|  |  |  |  |
| --- | --- | --- | --- |
| **Course Name:** | **Digital Electronics (116U02C304)** | **Semester:** | **III** |
| **Date of Performance:** |  | **Batch No:** |  |
| **Faculty Name:** |  | **Roll No:** |  |
| **Faculty Sign & Date:** |  | **Grade/Marks:** |  |

# Experiment No: 7 Title: Study of Asynchronous Counters

|  |
| --- |
| **Aim and Objective of the Experiment:** |
| 1. Implementation of decade counter using IC 7490.
2. Implement mod 6 counter using 7490
 |

|  |
| --- |
| **COs to be achieved:** |
| **CO3**: Design sequential circuits using MSI devices |

|  |
| --- |
| **Theory:** |
| * **Asynchronous counters**

In asynchronous counters universal clock is not used, only the first flip flop is driven by the main clock and the clock input of the rest of the flip flops is driven by output of previous flip flops. This can be seen in following diagram**Asynchronous Counter Circuit**In this circuit, Q0 is toggling on the rising edge of the clock pulse, Q1 is changing when the rising edge of Q0 is encountered (because Q0 is like clock pulse for second flip flop) and so on. In this way binary count is generated and ripples are created through Q0,Q1,Q2,Q3 hence it is also called RIPPLE counter. |

* **IC 7490**

IC 7490 is an asynchronous decade counter, which has mod 2 and mod 5 counter internally

**Block Diagram**

**Circuit Diagram/ Block Diagram:**

|  |
| --- |
| **Stepwise-Procedure:** |
| 1. Implement asynchronous decade counter using 7490.
2. Implement a mod 6 counter using IC 7490.
 |

|  |
| --- |
| **Post Lab Subjective/Objective type Questions:** |
| 1. **One of the major drawbacks to the use of asynchronous counters is that**

a : Low-frequency applications are limited because of internal propagation delays b : High-frequency applications are limited because of internal propagation delaysc : Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applicationsd : Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications1. **A counter is implemented using three (3) flip-flops, possibly it will have maximum output status.**

a : 3 , b : 7 , c : 8 , d : 151. Comment on limitation of frequency of asynchronous counters
2. Show how a Mod 6 counter can be designed using 3-bit asynchronous counter.
3. Design a 00 to 99 counter using IC 7490.
 |

**Conclusion:**

**Signature of faculty in-charge with Date:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Course Name:** | **Digital Electronics****116U02C304** | **Semester:** | **III** |
| **Date of Performance:** |  | **Batch No:** |  |
| **Faculty Name:** |  | **Roll No:** |  |
| **Faculty Sign & Date:** |  | **Grade/Marks:** |  |

**Experiment No: 9**

# Title: Synchronous counter

|  |
| --- |
| **Aim and Objective of the Experiment:** |
| 1. Implementation of 4-bit synchronous counter using MSI device (IC 74163)
2. 3 Bit Synchronous counter
 |

|  |
| --- |
| **COs to be achieved:** |
| **CO3:** Design sequential circuits using MSI devices**CO4:** Analyze and design synchronous sequential circuits using flip flops |

|  |
| --- |
| **Theory:** |
| **Synchronous Counter:** The circuit diagram of a 4-bit synchronous counter is shown in figure. In synchronous counter all the flip flops are clocked together. The speed of operation is better than ripple counter as clock is synchronous. From the truth table, the LSB A changes with every clock which can be achieved by giving J =K = 1 (assuming we use a JK FF). In second column, B changes whenever A changes from 1 to 0. So connect A to the inputs, J and K of next FF. similarly C changes when both A and B are 1. So J and K of C FF is A and B. Similarly, a change happens in D FF when A, B and C are high. So input to D is A and B and C.Since it is a 4 bit counter we require 4 FFs. One FF can store 1 bit. |
|  | D | C | B | A |  |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |



|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Load | ENT | ENP | CLR | CLK | Mode |
| 0 | X | X | 1 |  | Preset |
| 1 | 0 | 1 | 1 | X | stop count |
| 1 | X | 0 | 1 | X | stop count ,disableRC |
| X | X | X | 0 |  | Reset to 0 |
| 1 | 1 | 1 | 1 |  | Up count |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | 0 | 1 | 1 | 1 |  |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |
| Synchronous Counter: Definition, Working, Truth Table & Design74163 – 4bit synchronous counterFunction Table74163 has a synchronous clear and present. RC will be 1 when output reaches maximum count. |

|  |
| --- |
| **Synchronous Counter:** The circuit diagram of a 4-bit synchronous counter is shown in figure. In synchronous counter all the flip flops are clocked together. The speed of operation is better than ripple counter as clock is synchronous. From the truth table, the LSB A changes with every clock which can be achieved by giving J =K = 1 (assuming we use a JK FF). In second column, B changes whenever A changes from 1 to 0. So connect A to the inputs, J and K of next FF. similarly C changes when both A and B are 1. So J and K of C FF is A and B. Similarly, a change happens in D FF when A, B and C are high. So input to D is A and B and C.Since it is a 4 bit counter we require 4 FFs. One FF can store 1 bit. |
|  | D | C | B | A |  |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | 1 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |
| 74163 has a synchronous clear and preset. RC will be 1 when output reaches maximum count. |

|  |
| --- |
| **Stepwise-Procedure:** |
| 1. Implement 4-bit counter using 74163 IC
2. Implement mod 11 counter using 74163 (Make use of preset inputs)
3. Implement 8-bit counter using two 74163
4. Design the3 bit/ 4-bit synchronous counter on paper using JK FF
5. Connect the circuit on bread board/digital trainer
6. First reset the counter to 0 by giving clear input (clear =0 for JKFF 7476)
7. Keep the clear input high for counting
8. Verify the truth table for each clock
9. Using 74163 IC perform 4-bit counting
10. Implement 8-bit counter using two 74163
 |

|  |
| --- |
| **Post Lab Subjective/Objective type Questions:** |
| 1. Design a 3-bit binary synchronous up/down counter using T flip-flop and gates.
2. Design a Mod-5synchronous counter using JK flip-flop and gates.
3. Implement a mod 6 counter using a 4-bit synchronous counter IC
4. Design a 3-bit binary synchronous up/down counter using T flip-flop and gates.
5. Design a Mod-5synchronous counter using JK flip-flop and gates.
6. Implement a mod 6 counter using a 4-bit synchronous counter IC
7. What will be the counting sequence?

 |

**Conclusion:**

**Signature of faculty in-charge with Date:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Course Name:** | **Digital Electronics (116U02C304)** | **Semester:** | **III** |
| **Date of Performance:** |  | **Batch No:** |  |
| **Faculty Name:** |  | **Roll No:** |  |
| **Faculty Sign & Date:** |  | **Grade/Marks:** |  |

**Experiment No:8**

# Title: Study of Shift Registers

|  |
| --- |
| **Aim and Objective of the Experiment:** |
| 1. Design and Implementation of shift register using Flip Flop and MSI devices(IC 74194) |

|  |
| --- |
| **COs to be achieved:** |
| **CO3**: Design sequential circuits using MSI devices |

|  |
| --- |
| **Theory:** |
| * Shift Registers

In Serial In Parallel Out (SIPO) shift registers, the data is stored into the register serially while it is retrieved from it in parallel-fashion. Figure 1 shows an n-bit synchronous SIPO shift register sensitive to positive edge of the clock pulse. Here the data word which is to be stored (Data in) is fed serially at the input of the first flip-flop (D1 of FF1). It is also seen that the inputs of all other flip- flops (except the first flip-flop FF1) are driven by the outputs of the preceding ones like the input of FF2 is driven by the output of FF1. In this kind of shift register, the data stored within the register is obtained as a parallel-output data word (Data out) at the individual output pins of the flip-flops (Q1 to Qn). |

* Types of Inputs and Outputs

Depending on input and output of shift registers they are classified as Parallel In Serial Out (PISO), Serial In Parallel Out (SIPO) parallel In Parallel Out (PIPO) and Serial In Serial Out (SISO)

Whenever input or output is serial, the data will take number of clock cycles to be inputted or outputted hence the access time will depend on width of the shift register

* Left shift, Right Shift

When the number / data is shifted from LSB to MSB it is left shift and when it is shifted from MSB to LSB it is right shift.

In left shift we insert new bits from LSB, in right shift we insert new bits from MSB.

Since in positional numbers bits on left have more weight when the data is shifted left its value increases, when it is shifted right its value decreases.

Left Shift in Binary = Multiplication of 2 (Bit inserted is zero) Right shift in Binary = Division by 2 (Bit inserted is zero)

* Rotate, Ring counters

If we insert LSB to MSB in right shift or insert MSB in LSB in Left shift, then the same bits rotate and that is called as ring counter

* Universal Shift Registers IC 74194

The IC 74194 are high-speed Si-gate CMOS. The functional characteristics of the IC 74194 4-bit bidirectional universal shift registers are indicated in the logic diagram and function table. The registers are fully synchronous.

The synchronous operation of the device is determined by the mode select inputs (S0, S1). As shown in the mode select table, data can be entered and shifted from left to right (Q0 → Q1

→ Q2, etc.) or, right to left (Q3 → Q2 → Q1, etc.) or parallel data can be entered, loading all 4 bits of the register simultaneously.

When both S0 and S1 are LOW, existing data is retained in a hold (“do nothing”) mode. The first and last stages provide D-type serial data inputs (DSR, DSL) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode select and data inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The four parallel data inputs (D0 to D3) are D-type inputs. Data appearing on the D0 to D3 inputs, when S0 and S1 are HIGH, is transferred to the Q0 to Q3 outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous master reset (MR) overrides all other input conditions and forces the Q outputs LOW.

**Circuit Diagram/ Block Diagram:**

|  |
| --- |
| **Stepwise-Procedure:** |
| 1) Implement 4-bit Serial In Parallel out Shift Register using hardware. 2.) Implement 4-bit Parallel in Serial Out shift register using hardware.1. Implement a Ring counter using 4-bit Serial In Serial Out Shift register
2. Verify function table of IC 74194 and also implement a twisted ring counter using it
 |

|  |
| --- |
| **Post Lab Subjective/Objective type Questions:** |
| 1. **How can parallel data be taken out of a shift register simultaneously?**a : Use the Q output of the first FF b : Use the Q output of the last FF c : Tie all of the Q outputs togetherd : Use the Q output of each FF |

1. **The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains**

a : 01110

b : 00001

c : 00101

d : 00101

1. Make a MOD-5 Ring Counter using shift register in simulator
2. Using IC 74194 Universal Shift Register implement 8 bit Johnson counter

**Conclusion:**

**Signature of faculty in-charge with Date:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Course Name:** | **Digital Electronics (116U02C304)** | **Semester:** | **III** |
| **Date of Performance:** |  | **Batch No:** |  |
| **Faculty Name:** |  | **Roll No:** |  |
| **Faculty Sign & Date:** |  | **Grade/Marks:** |  |

**Experiment No: 10**

# Title: Vending machine

|  |
| --- |
| **Aim and Objective of the Experiment:** |
| 1. Design a vending machine which accepts Rs. 10 and Rs. 20. The machine dispose soft drink for Rs.50 and returns balance if any. Design as mealy machine |

|  |
| --- |
| **COs to be achieved:** |
| **CO4:** Analyze and design synchronous sequential circuits using flip flops |

|  |
| --- |
| **Theory:** |
| **Mealy machine**In the theory of computation, a Mealy machine is a finite-state machine whose output values are determined both by its current state and the current inputs. A Mealy machine is a deterministic finite state transducer: for each state and input, at most one transition is possible.**Moore machine**A Moore machine is a finite-state machine whose output values are determined solely by its current state. This is in contrast to a Mealy machine, whose output values are determined both by its current state and by the values of its inputs.**Vending Machine,** a machine that dispenses small articles such as food, drinks, or cigarettes when a coin or token is inserted. |

|  |
| --- |
| **Stepwise-Procedure:** |
| 1. Draw the state diagram.
2. Write the state table.
3. Design using JK flip flops and gates
 |

|  |
| --- |
| **Post Lab Subjective/Objective type Questions:** |
| A clocked synchronous sequential should have an output z=1, if the total number of zeros received is an odd number greater than 1, provided that two consecutive ones have never been received. Design the machine using minimum risk approach method and T FF |

**Conclusion:**

**Signature of faculty in-charge with Date:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Course Name:** | **Digital Electronics (116U02C304)** | **Semester:** | **III** |
| **Date of Performance:** |  | **Batch No:** |  |
| **Faculty Name:** |  | **Roll No:** |  |
| **Faculty Sign & Date:** |  | **Grade/Marks:** |  |

**Experiment No: 11 Title: Characterization of logic families – Virtual Labs**

|  |
| --- |
| **Aim and Objective of the Experiment:** |
| Use virtual labs provided by IIT Kharagpur to characterize TTL NAND and CMOS NAND gates |

|  |
| --- |
| **COs to be achieved:** |
| **CO5:** Understand characteristics of different logic families and semiconductor devices. |

|  |
| --- |
| **Theory:** |
| Refer the following link:[http://vlabs.iitkgp.ernet.in/dec/#](http://vlabs.iitkgp.ernet.in/dec/) |

|  |
| --- |
| **Stepwise-Procedure:** |
| Write the procedure |

**Post Lab Subjective/Objective type Questions:**

Explain VIL, VIH, VOL,VOH

**Conclusion:**

**Signature of faculty in-charge with Date:**